AMENDMENTS TO THE CLAIMS

1.-24. (Cancelled)

25. (Currently Amended) The circuit arrangement according to Claim 29, wherein the storage flip-flop subcircuit has two inverters formed from the storage transistors.

26. (Withdrawn) The circuit arrangement according to Claim 29, wherein the first power switch transistor is a common power switch transistor provided for the flip-flop and for at least one additional flip-flop.

27. (Currently Amended) The circuit arrangement according ~~to one of~~ Claim 29, wherein the thickness of a gate insulating layer of the storage transistors and/or of the first power switch transistor is greater than the thickness of the gate insulating layer of the switching transistors.

28. (Previously Presented) The circuit arrangement according to Claim 29, wherein a channel width of the storage transistors and/or of the first power switch transistor is less than the channel width of the switching transistors.

29. (Currently Amended) A circuit arrangement comprising:

an edge-triggered flip-flop, comprising:

a storage flip-flop subcircuit having a plurality of storage transistors with a threshold voltage of a first value;

a first power switch transistor having a threshold voltage of a second value, wherein an application of a predetermined electrical potential to the first power switch transistor's gate terminal brings the circuit arrangement to an operating state in which if at least one supply voltage is switched off, electric charge carriers contained in the circuit arrangement are prevented from discharging from the circuit arrangement;

a plurality of switching transistors, having a threshold voltage of a third value, provided between the storage flip-flop subcircuit and the first power switch transistor, for coupling a flip-flop input signal into the storage flip-flop subcircuit wherein each of the terminals of the switching transistors has a defined electrical potential in the operating state;

a pulse generator circuit that generates a flip-flop input signal from an input signal and from a clock signal and is coupled to the first power switch transistor and to the switching transistors; and

wherein the magnitude of the first and/or the second value is greater than the magnitude of the third value.

30. (Previously Presented) The circuit arrangement according to Claim 29, having at least one second power switch transistor, which is coupled to at least a portion of the switching transistors such that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, a gate terminal of each of the switching transistors coupled to the at least one second power switch transistor has a defined electrical potential.

31. (Currently Amended) The circuit arrangement according to Claim 29, having at least one second power switch transistor~~, 602~~, which is coupled to at least a portion of the switching transistors such that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, a source/drain terminal of each of the switching transistors coupled to the at least one second power switch transistor has a defined electrical potential.

32. (Previously Presented) The circuit arrangement according to Claim 31, wherein the second power switch transistor is a p-MOS field effect transistor.

33. (Cancelled)

34. (Currently Amended) The circuit arrangement according to Claim 29 [[33]], wherein the pulse generator circuit comprises a plurality of pulse generator transistors having a threshold voltage of a fourth value, wherein the magnitude of the first and/or the second value is greater than the magnitude of the fourth value.

35. (Currently Amended) The circuit arrangement according to Claim 34 [[33]], wherein the pulse generator circuit comprises a logic subcircuit that generates at least one flip-flop input signal from at least one input signal in accordance with a predetermined logic operation.

36. (Previously Presented) The circuit arrangement according to Claim 35, wherein the logic subcircuit operates as one of an inverter, AND gate, OR gate, NAND gate, NOR gate, exclusive OR gate, and exclusive NOR gate.

37. (Previously Presented) The circuit arrangement according to Claim 36, wherein the logic subcircuit comprises a plurality of logic transistors having a threshold voltage of a fourth value, wherein the magnitude of the first and/or the second value is greater than the magnitude of the fourth value.

38. (Cancelled)

39. (Currently Amended) The circuit arrangement according to Claim 37, further comprising a test circuit coupled to the storage flip-flop subcircuit, wherein the test circuit tests the functionality of the storage flip-flop subcircuit.

40. (Currently Amended) The circuit arrangement according to Claim 39, wherein the test circuit has an input component that programs a test input signal into [[of]] the storage flip-flop subcircuit, and an output component that reads out a test output signal from [[of]] the storage flip-flop subcircuit.

41. (Previously Presented) The circuit arrangement according to Claim 39, wherein the test circuit has a plurality of test transistors with a threshold voltage having a fifth value, wherein the magnitude of the fifth value is greater than at least one of the magnitudes of the third to fourth values.

42. (Previously Presented) The circuit arrangement according to Claim 41, wherein the test transistors have a gate insulating layer having a thickness greater than a thickness of the gate insulating layer of the switching transistors.

43. (Previously Presented) The circuit arrangement according to Claim 41, wherein the test transistors have a gate insulating layer having a thickness greater than a thickness of a gate insulating layer of the pulse generator transistors.

44. (Previously Presented) The circuit arrangement according to Claim 41, wherein the test transistors have a gate insulating layer having a thickness greater than a thickness of a gate insulating layer of the logic transistors.

45. (Currently Amended) The circuit arrangement according to Claim 29, further comprising one or more protection transistors having a threshold voltage of a fourth value and located between the storage flip-flop subcircuit and the switching transistors, wherein the protection transistors selectively couple or decouple the storage flip-flop subcircuit and the switching transistors, and the magnitude of the fourth value is greater than the magnitude of the third value.

46. (Previously Presented) The circuit arrangement according to Claim 45, wherein the protection transistors have a gate insulating layer having a thickness greater than a thickness of the gate insulating layer of the switching transistors.

47. (Currently Amended) The circuit arrangement according to Claim 34, further comprising one or more protection transistors having a threshold voltage of a

fifth value and located between the storage flip-flop subcircuit and the switching transistors, wherein the protection transistors selectively couple or decouple the storage flip-flop subcircuit and the switching transistors, and the magnitude of the fifth value is greater than the magnitude of the third value, and

wherein the protection transistors have a gate insulating layer having a thickness greater than a thickness of the gate insulating layer of the pulse generator transistors.

48. (Currently Amended) The circuit arrangement according to Claim 37, further comprising one or more protection transistors having a threshold voltage of a fifth value and located between the storage flip-flop subcircuit and the switching transistors, wherein the protection transistors selectively couple or decouple the storage flip-flop subcircuit ~~hp-flop~~ and the switching transistors, and the magnitude of the fifth value is greater than the magnitude of the third value, and

wherein the protection transistors have a gate insulating layer having a thickness greater than the thickness of a gate insulating layer of the logic transistors.

49. (Currently Amended) The circuit arrangement according to Claim 45, wherein

in a first operating state, when at least one supply voltage of the circuit arrangement is switched off, by applying electrical control signals to at least a portion of the protection transistors, the protection transistors electrically decouple the storage flip-flop subcircuit and the switching transistors from one another; and

in a second operating state, when supply voltages are applied to the circuit arrangement, by applying electrical control signals to at least a portion of the protection ~~switching~~ transistors, the protection ~~switching~~ transistors electrically couple the storage flip-flop subcircuit and the switching transistors to one another.

50. (Currently Amended) The circuit arrangement according to Claim 45, wherein the protection transistors have at least one transistor pair of transistors of different conduction types connected in parallel with one another, and at least one transistor pair connected by its source/drain terminals between the storage flip-flop subcircuit and the switching transistors.

51. (Currently Amended) A circuit arrangement comprising:

an edge-triggered flip-flop, comprising:

a storage flip-flop subcircuit having a plurality of storage transistors with a threshold voltage of a first value;

~~at least one additional flip-flop having a plurality of storage transistors with a threshold voltage of the first value;~~

a ~~first~~ power switch transistor having a threshold voltage of a second value, wherein an application of a predetermined electrical potential to the ~~first~~ power switch transistor's gate terminal brings the circuit arrangement to an operating state in which if at least one supply voltage is switched off, electric charge carriers contained in the circuit arrangement are prevented from discharging from the circuit arrangement; and

a plurality of switching transistors, having a threshold voltage of a third value, provided between the storage flip-flop subcircuit and the ~~first~~ power switch transistor, for coupling a flip-flop input signal into the storage flip-flop subcircuit;

wherein the magnitude of the first and/or the second value is greater than the magnitude of the third value; and

a pulse generator circuit that generates a flip-flop input signal from an input signal and from a clock signal and is coupled to the ~~first~~ power switch transistor and to the switching transistors;

at least one additional edge-triggered flip-flop; ~~and~~

wherein the ~~first~~ power switch transistor is ~~a power switch transistor~~ provided for the edge-triggered flip-flop and for the at least one additional edge-triggered flip-flop.

52. (Currently Amended) A circuit arrangement comprising:

an edge-triggered flip-flop, comprising:

a storage flip-flop subcircuit having a plurality of storage transistors with a threshold voltage of a first value;

a first power switch transistor having a threshold voltage of a second value, wherein an application of a predetermined electrical potential to the first power switch transistor's gate brings the circuit arrangement to an operating state in which if at least one supply voltage is switched off, electric charge carriers contained in the circuit arrangement are prevented from discharging from the circuit arrangement;

a plurality of switching transistors, having a threshold voltage of a third value, provided between the storage flip-flop subcircuit and the first power switch transistor, for coupling a flip-flop input signal into the storage flip-flop subcircuit wherein at least one of the terminals of the switching transistors has a defined electrical potential in the operating state;

wherein the magnitude of the first and/or the second value is greater than the magnitude of the third value;

a pulse generator circuit that generates a flip-flop input signal from an input signal and from a clock signal and is coupled to the first power switch transistor and to the switching transistors; and

at least one second power switch transistor, which is coupled to at least a portion of the switching transistors such that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, a gate terminal of each of the switching transistors coupled to the at least one second power switch transistor has a defined electrical potential.

53. (Currently Amended) A circuit arrangement comprising:

an edge-triggered flip-flop, comprising:

a storage flip-flop subcircuit having a plurality of storage transistors with a threshold voltage of a first value;

a first power switch transistor having a threshold voltage of a second value, wherein an application of a predetermined electrical potential to the first power switch transistor's gate terminal binges the circuit arrangement to an operating state in which if at least one supply voltage is switched off, electric charge carriers contained in the circuit arrangement are prevented from discharging from the circuit arrangement;

a plurality of switching transistors, having a threshold voltage of a third value, provided between the storage flip-flop subcircuit and the first power switch transistor, for coupling a flip-flop input signal into the storage flip-flop subcircuit wherein at least one of the terminals of the switching transistors has a defined electrical potential in the operating state;

wherein the magnitude of the first and/or the second value is greater than the magnitude of the third value;

a pulse generator circuit that generates a flip-flop input signal from an input signal and from a clock signal and is coupled to the first power switch transistor and to the switching transistors; and

at least one second power switch transistor, which is coupled to at least a portion of the switching transistors such that, in an operating state of the circuit arrangement in which at least one supply voltage of the circuit arrangement is switched off, a source/drain terminal of each of the switching transistors coupled to the at least one second power switch transistor has a defined electrical potential.